


I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

PATENT
Attorney Docket No.: 20865-000121US

Assistant Commissioner for Patents
Washington, D.C. 20231

On _____

TOWNSEND and TOWNSEND and CREW LLP

By: 

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

G. Ramanath, et al.

Application No.: 09/977,069

Filed: October 11, 2001

For: SELF-ASSEMBLED NEAR-ZERO-
THICKNESS MOLECULAR LAYERS
AS DIFFUSION BARRIERS FOR CU
METALLIZATION

Examiner: Erik Kielin

Art Unit: 2813

DECLARATION OF SHYAM MURARKA
PURSUANT TO 37 C.F.R. § 1.132

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Shyam Murarka, reside at 7 Shadowbrook Dr., Clifton Park, NY 12065, and declare as follows:

1. A brief discussion of my background is attached hereto as Exhibit A. As shown in Exhibit A, I have extensive experience in the fields of microelectronics and materials science.
2. I am a co-inventor in the present patent application.
3. I have reviewed the present application, the attached Amendment including new claims 6-20, the Office Action mailed August 21, 2002, and U.S. Patent Nos. 5,079,600 (Schnur '600) and 5,389,496 (Calvert '496).

4. On page 3 of the Office Action, claims 1-5 were rejected as being anticipated by Schnur '600. The Office Action states "Schnur discloses a diffusion barrier (Fig. 1A, called 'thin film') in an integrated circuit (Abstract). ... It is seen to be inherent that the 'thin film' is a diffusion barrier, because it is the same material as that disclosed by Applicant, and because a 'metal' film is formed on the 'thin film' and is shown in the Schnur figures not to be diffused through the thin film SAM, thereby meeting Applicant's definition of 'diffusion barrier'".

5. On page 4 of the Office Action, claims 1-5 are rejected as anticipated by Calvert '496. The rejection states "it is seen to be inherent that the covalently bonded 'chemical groups' or 'catalyst ligating groups' of Calvert inherently form a self-assembled monolayer which serves as a diffusion barrier layer for the reasons indicated above in reference to Schnur."

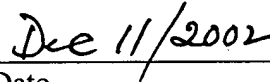
6. Contrary to the assumption in the rejections based on Schnur '600 and Calvert '496, I do not believe that either reference "inherently" discloses a "diffusion barrier". Neither Schnur '600 nor Calvert '496 describe or suggest self-assembled monolayers that are diffusion barriers. For example, neither Schnur '600 nor Calvert '496 tested their structures like the present inventors to show that copper diffusion does not occur under conditions such as thermal bias annealing. Consequently, I do not believe that the inventions defined by claims 6-20, each of which recites a "diffusion barrier", in the Amendment are "inherent" in Schnur '600 or Calvert '496.

7. I believe that the embodiments of the invention that are described in the present application also provide evidence of unexpected results. As shown in Figure 3 of the present application and as suggested at paragraph 25 of the present application, the present inventors have discovered that self-assembled monolayers (SAMs) with molecules with longer chains and aromatic terminal groups are better at preventing diffusion than SAMs with molecules having shorter chains and aliphatic terminal groups. Neither Schnur '600 nor Calvert '496 recognize that SAMs with molecules having longer chains and aromatic terminal groups are better at preventing diffusion than SAMs with molecules having shorter chains and aliphatic terminal groups.

8. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-referenced application or any patent issuing thereon.



Shyam Murarka, Ph.D.



Date

Exhibit A: BACKGROUND OF SHYAM P. MURARKA

SHYAM P. MURARKA has recently (September, 2002) retired. He was the Elaine S. and Jack S. Parker Chair in Engineering and a Professor in the Center for Integrated Electronics, Electronics Manufacturing and Electronic Media (CIEEM) and Materials Science and Engineering Department. He received a Ph.D. degree in Chemistry from Agra University, Agra, India, in 1970, and a Ph.D. degree in Metallurgy and Materials Science from the University of Minnesota, Minneapolis, also in 1970.

Prior to joining Rensselaer, from 1972 until August 1984, he had been with Bell Laboratories, Murray Hill, NJ, where he received a Distinguished Technical Staff Award (in 1992, the first time such awards were made) and was a Supervisor in the Materials Technology Department. He was the Director of the Center for Advanced Interconnect Science and Technology (CAIST) from 1996-2000 and was responsible for the NY Focus Research Center (FRC) program at Rensselaer 1997-1998. He was an FRC advisory council member. He was Director of CIEEM from July 1994 until April 1996 and Co-Director of SEMATECH Center of Excellence at Rensselaer Polytechnic Institute from January 1990 until August 1996. He has been a member of several professional societies and received the 1987 Thomas D. Callinan Award and the 2001 Electronics Division Award, both of the Electrochemical Society and became a fellow of American Society of Metals, International in 1991, of American Vacuum Society in 1993, of IEEE in 1995 and of ECS in 1997. Also, he has been a member of several nationwide panels (e.g., SIA NTRS Roadmap, NSF-New Paradigms for Manufacturing 1994, Micro Tech 2000, 1991, etc.) to discuss advanced technology issues in microelectronics. As a frequent contributor to technical publications in the field of Materials Science, he has published over 260 papers and given over 270 talks (about half invited) on the diffusion and defects in metals, oxides, and semiconductors; thin films and thin film metallization of IC's and has written books, "Silicides for VLSI Applications", (Academic Press, NY, 1983); "Electronics Materials, Science and Technology" with Dr. M. Peckerar (Academic Press, 1989), "Metallization Theory and Practice for VLSI and ULSI", (Butterworth, 1993), "Chemical Mechanical Planarization of Microelectronic Materials", (Wiley, 1997) with Drs. J. Steigerwald and R. Gutmann, and "Copper: Fundamental Mechanisms for Microelectronic Applications," (Wiley, 2000) with Drs. I. V. Verner and R. J. Gutmann. He also has co-edited three books on "Advanced Metallization in Microelectronics", (MRS 1990, 1992, 1994), one on "Interface Control of Electrical, Chemical, and Mechanical Properties", (MRS 1994), one on "Microelectronics Technology and Process Integration", (SPIE, 1994), and one on "Low Dielectric Constant Materials -Synthesis and Applications in Microelectronics" (MRS, 1995), and one on "Advanced Interconnects and Contact Materials and Processes for Future Integrated Circuits," (MRS, 1998), and written review chapters in several edited volumes (books). He is presently actively involved with graduate students working in the area of multilevel interconnections specifically high conductivity metals, low dielectric constant interlayer dielectric, and planarization.

He had been a member of ASM International, The Electrochemical Society, IEEE, AVS, and MRS. He was also an Associate Editor of the Journal of Electrochemical Society and is frequent reviewer of the national and international journal articles. He has also co-edited special journal issues covering the interconnection issues in semiconductors.